

SHEET INDEXSYMBOL

ADDRESS & DATA
ELEMENT B

MANUFACTURING REFERENCES

SHEET INDEX NOTES

- NOTES:

- ### 3. BATTERY AND GROUND TERMINALS FOR INTEGRATED CIRCUITS

IC CODE	BAY. TERM.	GRD. TERM.
144AJ	1.38	19.20
153A	14	1

6. CMS 153A IS CONTROLLED BY CPS FC200.

RECORD OF CHANGES			
PREV FURN	STD	MFR DISC	SEE NOTE

SYSTEM USED ON	DESIGN CONTROL
COMMON SYSTEMS	IN

10015

1198

AT&T
STANDARD

SHEETS 9

1994

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PART OF CPS FC203

CLOCK CIRCUIT

COMPONENT LIST

CAPACITOR

DESIG	CODE
[2] C1-C7	K5-20013 L4, 42, 20PF
C8	K5-19714 L1, .01
C9	K5-19714 L1, 1000PF
C10	K5-20013 L4, 316PF
[3] C11-C13	K5-20013 L4, 215PF
	K5-19714 L4, .1

CRYSTAL

DESIG	CODE
[1] Y1	106A5 14, 9254

DIODE

DESIG	CODE
[3] CR1-CR3	458A
CR4	458C

INDUCTOR

DESIG	CODE
L1	K5-13726 L76, 4.22uH
L2	K5-13726 L24, 33uH

INTEGRATED CIRCUIT

DESIG	CODE
CH1	16A8J
CH2	153A

RESISTOR

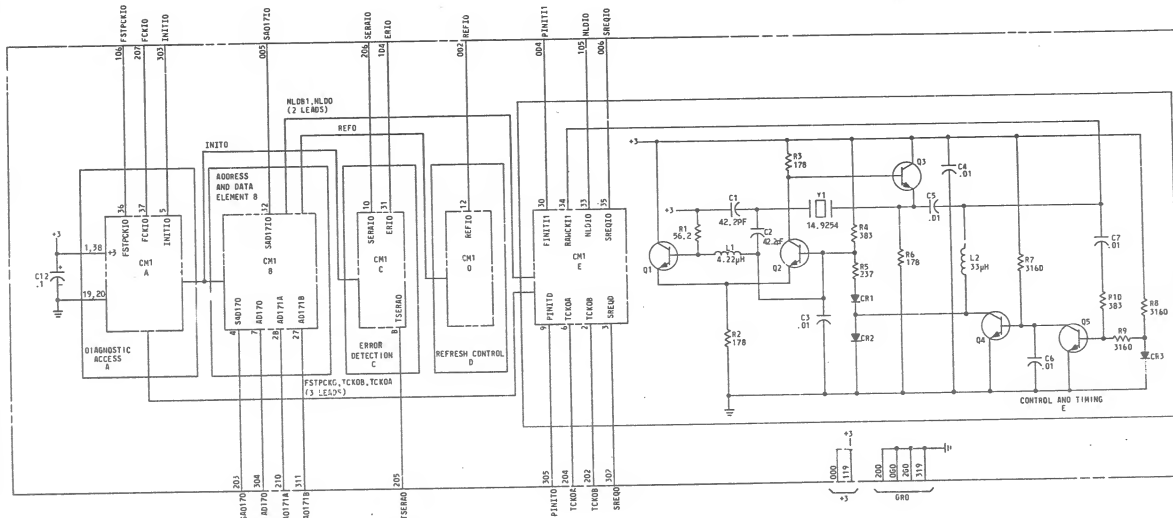
DESIG	CODE
[2] R1	K5-20616 L14, 96, 2
R2	175
R3	363
R4	237
[3] R5-R9	170
R10	3160
R11	511
R12	2150
R13	1210
R14	16, 7
R15	2370
R16	237
R17	K5-20616 L14, 3870

TRANSFORMER

DESIG	CODE
[4] T1-T4	26A80

TRANSISTOR

DESIG	CODE
[3] Q1-Q3	45A
Q4	46J



2A

FC203 CIRCUIT PAGE

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CPS-FC203

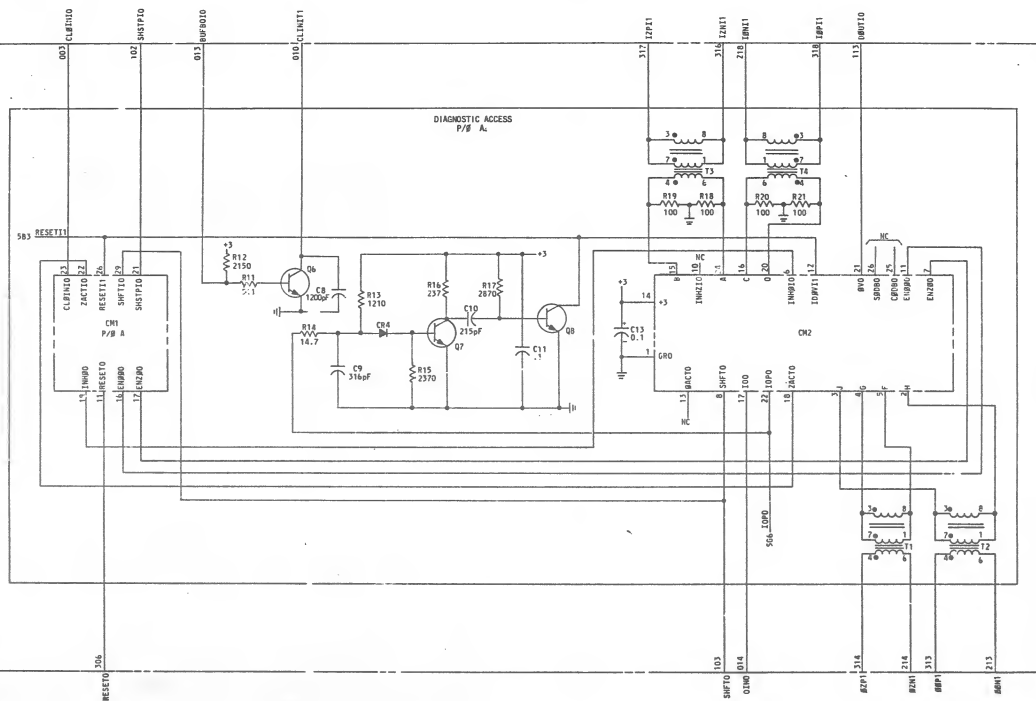
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BELL TELEPHONE LABORATORIES

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PRINTED IN U.S.A.

PART OF CPS FC203 CLOCK CIRCUIT



PART OF CPS FC 203 CLOCK TIMING

CIRCUIT DESCRIPTION

A. FUNCTION

THE FC203 IS A CLOCK CIRCUIT PACK USED IN THE MAIN STORE CONTROLLER CIRCUIT (MASC). IT CONTAINS THE INTERFACE AND CONTROL CIRCUITS WHICH ENABLE COMMUNICATION WITH THE MAIN STORE CONTROL (MSC) OVER THE SERIAL I/B CHANNEL (SIBC). IT ALSO CONTAINS THE MASC CLOCK OSCILLATOR AND ASSOCIATED CONTROLS, ONE BIT OF THE STORE ADDRESS REGISTER, AND AN ERROR REGISTER (ER) BIT.

B. DETAILED DESCRIPTION

NET NAME CONVENTIONS

A CONVENTION HAS BEEN CHOSEN AND USED FOR NET NAME MNEMONICS:

- 1) THE LAST DIGIT OF A MNEMONIC WILL BE EITHER 1 OR 0, INDICATING THE ACTIVE VOLTAGE LEVEL (HIGH OR LOW, RESPECTIVELY) OF THAT NET. E.G., NET SEL0 IS ACTIVE WHEN VOLTAGE LOW.
- 2) IF THE LETTER IMMEDIATELY BEFORE THE LAST DIGIT IS AN I, THIS NET SERVES AS A SIGNAL INPUT TO THE CIRCUIT. E.G., SEL0 IS AN INPUT, WHILE SEL0 IS NOT.
- 3) IF THE LAST CHARACTER OF A NET NAME IS A LETTER, THIS NET IS A MEMBER OF A PARALLEL GROUP OF NETS CARRYING THE SAME SIGNAL. E.G., SEL0, SEL00, AND SEL000 WOULD BE THREE PARALLEL NETS, CARRYING THE SAME INFORMATION.
- 4) IF THE LETTER IMMEDIATELY BEFORE THE LAST DIGIT IS A B, THIS NET SERVES AS A SERIAL DUPLICATION OF THE NET WITHOUT THE B. E.G., SEL0 IS THE SERIAL DUPLICATE OF SEL0. SEL000 IS THE SERIAL DUPLICATE OF SEL00, ETC.
- 5) THE OUTPUTS OF A HIGH-LEVEL REGISTER, I.E., A 2-BIT REGISTER OR GATED DELAY FLIP-FLOP, UNLESS OTHERWISE REMARKED, WILL BE ACTIVE IF THE REGISTER IS SET. E.G., IF NET ER01 IS THE 01 OUTPUT OF REGISTER 0, THEN ER01 WILL BE ACTIVE IF REGISTER 0 IS SET. IF THIS NET IS MARKED ER000, THE NET WILL BE ACTIVE ONLY IF REGISTER 0 IS CLEARED.
- 6) IF THE FIRST CHARACTER OF A NET NAME IS THE LETTER T, THIS NET WILL BE A COLLECTOR-TYPE OUTPUT FROM TWO OR MORE GATES TIED TO THE SAME NET. E.G., TSEL0 IS SUCH A NET.

WHILE THESE CONVENTIONS HAVE BEEN CONSCIENTIOUSLY FOLLOWED, THERE WERE CIRCUMSTANCES THAT PRECLUDED THEIR USE. IN SUCH CASES, THE NET WILL BE SPECIALLY NOTED.

C. SYMBOL/LEAD MNEMONICS

MNEMONICS

DEFINITION

A0170	ADDRESS BIT 17 (OUTPUT)
A017A	ADDRESS BIT 17 (OUTPUT TO BRANCH A)
A017B	ADDRESS BIT 17 (OUTPUT TO BRANCH B)
B0F006	BUFFER BIT 0
CLIKI01	CLEAR INITIALIZE
CLIKI00	CLEAR THE CHANNEL ONE INHIBIT
00U010	DATA OUT (TO SIBC FROM MASC)
ER010	ERROR A REGISTER (INPUT)
FKC10	FORCE CLOCK (DIAGNOSTIC INPUT)
FSTPCK10	FORCE STOP CLOCK (DIAGNOSTIC INPUT)
05A0170	ADDRESS BIT 17 (OUTPUT TO HIGHER ORDER STORES)
05A000	STORE REQUEST (OUTPUT TO HIGHER STORES)
100	INPUT DATA (FROM SIBC TO MASC)
IKI010	INITIALIZE
IN011	INPUT ONE, NEGATIVE (SIBC INPUT TO MASC NEGATIVE FROM CHANNEL ONE)
INP011	INPUT ONE, POSITIVE (SIBC INPUT TO MASC POSITIVE FROM CHANNEL ONE)
IZ001	INPUT ZERO, NEGATIVE (SIBC INPUT TO MASC NEGATIVE FROM CHANNEL ZERO)
IZP011	INPUT ZERO, POSITIVE (SIBC INPUT TO MASC POSITIVE FROM CHANNEL ZERO)
HL010	NORMAL LOG0
00N01	OUTPUT ONE, NEGATIVE (SIBC OUTPUT FROM MASC NEGATIVE TO CHANNEL ONE)
00P01	OUTPUT ONE, POSITIVE (SIBC OUTPUT FROM MASC POSITIVE TO CHANNEL ONE)
02N01	OUTPUT ZERO, NEGATIVE (SIBC OUTPUT FROM MASC NEGATIVE TO CHANNEL ZERO)
02P01	OUTPUT ZERO, POSITIVE (SIBC OUTPUT FROM MASC POSITIVE TO CHANNEL ZERO)
PINI010	POWER INITIALIZE INPUT
PINI00	POWER INITIALIZE OUTPUT
REF010	REFRESH
REF0	REFRESH MODE
RESE00	RESET OF I/B FUNCTIONS
SA01710	ADDRESS BUS BIT 17 (INPUT)
SEK010	STORE ERROR A (FROM HIGHER STORES)
SHF010	SHIFT
SHFT0	SHIFT (SIBC SHIFT SIGNAL)
SHFTP0	SHIFT STOP
SR0010	STORE REQUEST
TC00A	CLOCK BRANCH A
TC00B	CLOCK BRANCH B
TSER00	STORE ERROR A OUTPUT

FC203 CIRCUIT PACK

BELL TELEPHONE LABORATORIES
INCORPORATED

CPS-FC203

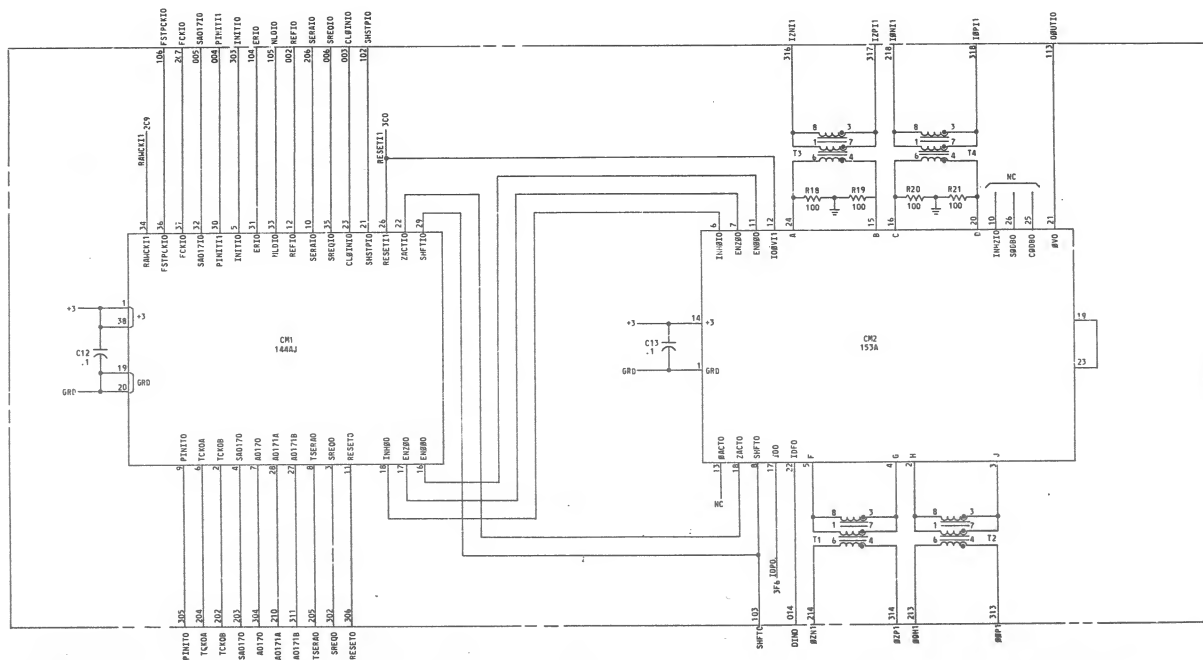
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REVISION 6A

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PART OF CPS FC 203

GENERAL BLOCK INTERCONNECTIONS



FC203 CIRCUIT PACK

BELL TELEPHONE LABORATORIES
INCORPORATED

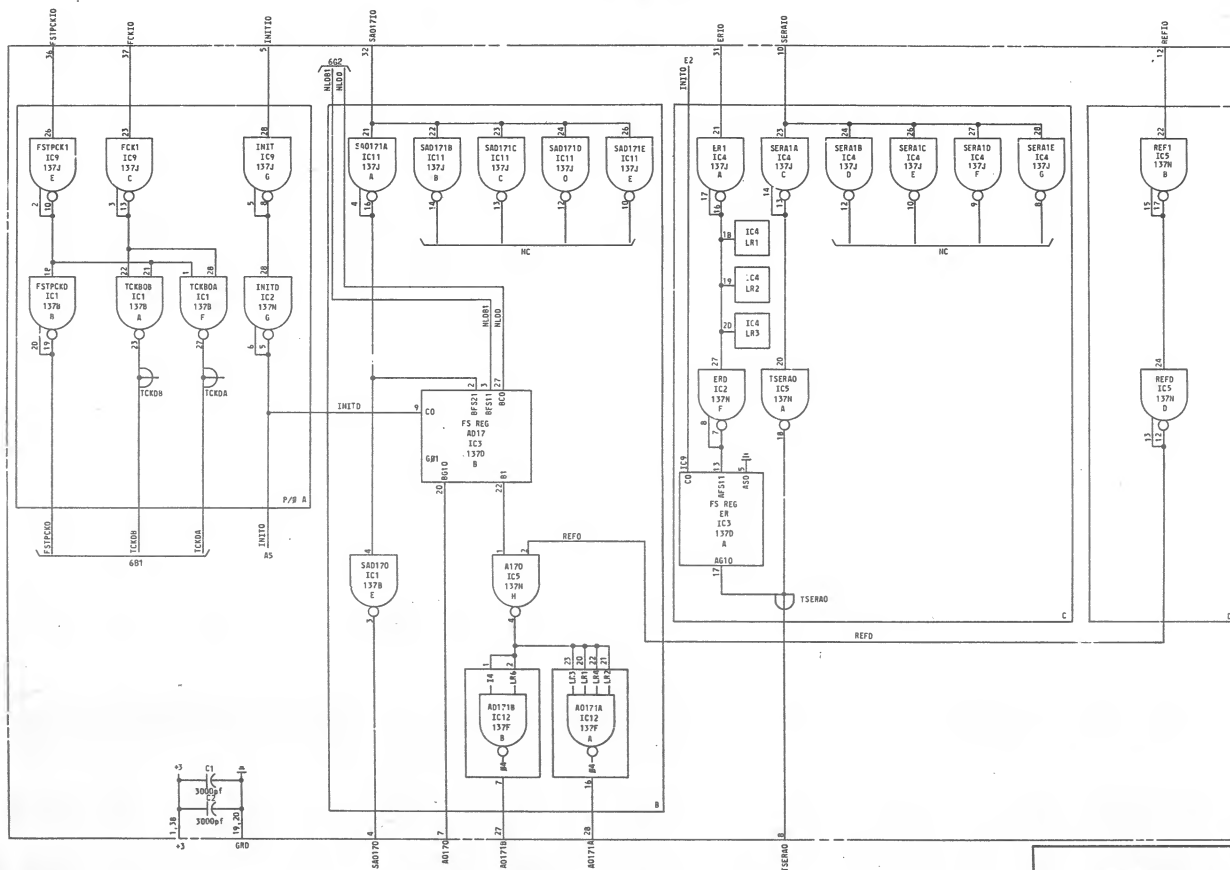
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CPS-FC203

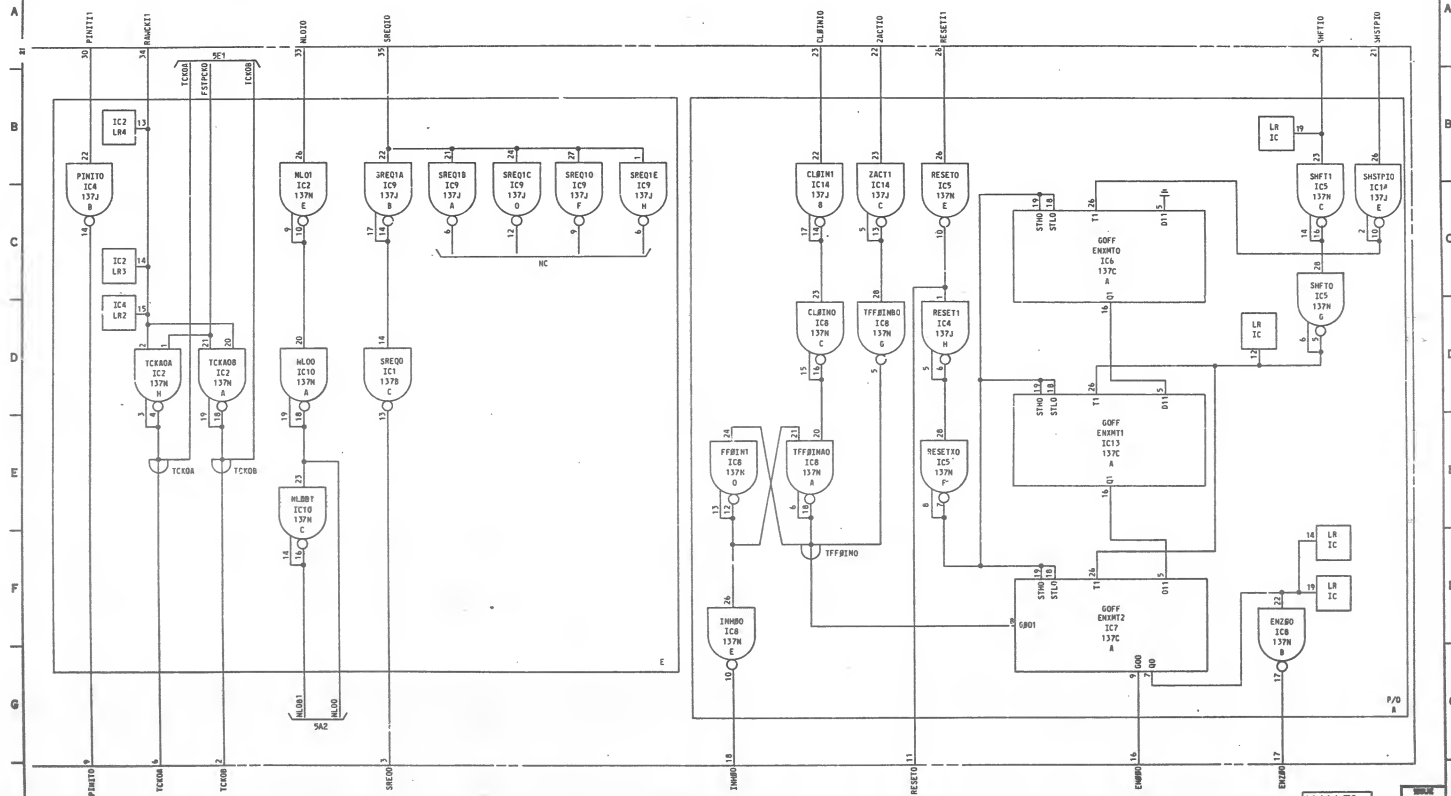
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PART OF CMS 144AJ



PART OF CMS 144AJ



PART OF CMS 144AJ

COMPONENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 137B	IC2 137N	IC3 137D	IC4 137J	IC5 137H	IC6 137C	IC7 137E	LOC CODE ELEM ID
DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	
A	TCR008	5C1	TCR008	601	ERAD17	503	PIN1TD	600
B	FSTPC0D	5C0			ER1	585	TSERAD	505
C	SREOC	602			PIN1TD	600	REF1	500
D					SERAD1	585	SHFT1	609
E	SAD1TD	5F2	NLD1	602	SERAD1	586	REF2	508
F	TCR00A	5C1	ERD	505	SERAD1	586	RESETO	606
G			THTD	5C2	SERAD1	587	RESETO	605
H			TCR00A	600	THTD	587	SHFT2	609
					RESETO	606	RESETO	609
					RESETO	606	RESETO	609

LOC CODE ELEM ID	IC8 137N	IC9 137J	IC10 137H	IC11 137J	IC12 (NOTE 1) 137F	IC13 137C	IC14 137J	LOC CODE ELEM ID
DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	DESIG	SH LOC	
A	177FBNB0	6E5	SREQ18	603	NLD0	601	SAD171A	502
B	ENR0D	6F8	SREQ18	602			AD171A	503
C	CLRW1D	605	FCR1	501			AD171B	503
D	FFELM1	6E5	SREQ1C	603			CLRW1	605
E	THWD	6F5	FSTPC1	500			ZACT1	606
F			SREQ1D	604			SHSTPIC	609
G	177FBNB0	606	INT1	502				
H			SREQ1E	604				

CAPACITOR

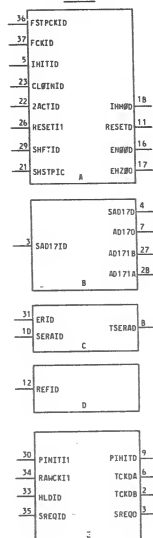
DESIG	CODE
(2) C1-C2	801A, 3000pF

NOTES:

1. A CAPACITOR CHIP (801A, 3000pF) IS MOUNTED ON EACH SIDE OF THE 137F SIC.

CIRCUIT DESCRIPTION

SYMBOL



BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT MODULE

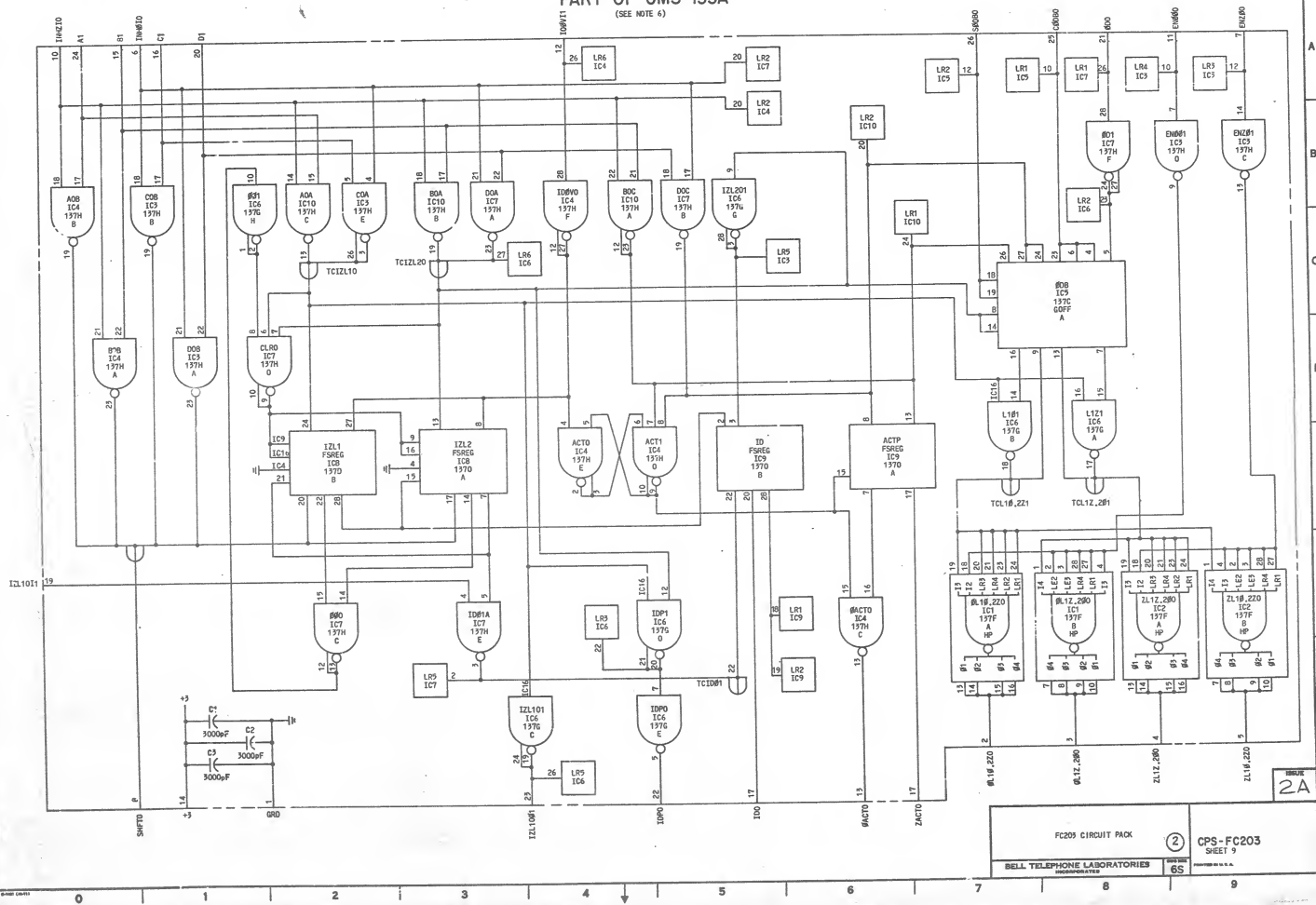
IC CODE	BAT TERM	GRD TERM
137B	25	11
137C	25	11
137D	25	11
137E	25	11
137F	25	11
137G	25	11
137H	25	11
137J	25	11

SUPPORTING INFORMATION

CATEGORY	NO.	FC203 CIRCUIT PACK	144AJ IC
INTEGRATED CIRCUIT CODE	144AJ		
ONLY ACCEPTABLE SERIES	6		
		BELL TELEPHONE LABORATORIES	CPS-FC203 SHEET 8

PART OF CMS 153A

(SEE NOTE 4)



PART OF CMS 153A

(SEE NOTE 6)

COMMENT LIST

INTEGRATED CIRCUIT

LOC CODE ELEM ID	IC1 1377 (NOTE 1)	IC2 1377 (NOTE 1)	IC3 137H	IC4 137H	IC5 137C	IC6 137D	IC7 137H	IC8 137D	IC9 137D	IC10 137H	LOC CODE ELEM ID
DES16	SH LOC	DES16	SH LOC	DES16	SH LOC	DES16	SH LOC	DES16	SH LOC	DES16	SH LOC
A	HL19.220	BF7	2L12.280	BF8	DOB	801	808	800	808	808	A
B	HL12.280	CF8	2L19.220	BF9	COB	801	808	800	808	808	B
C					EN2B1	889	889	889	889	889	C
D					EN2B1	889	889	889	889	889	D
E					CM	882	882	882	882	882	E
F					BACTO	8F5	8F5	8F5	8F5	8F5	F
G					10PVO	884	884	884	884	884	G
H											H

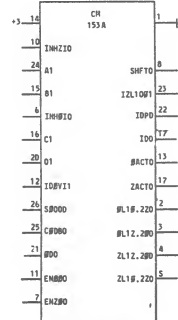
CAPACITORS

DES16	CODE
137 C1-C3	801 A 2000 Pf

NOTES:

1. A CAPACITOR CHIP (801 A, 2000 Pf) IS BONDED ON EACH SIDE OF THE 137 F SIC.

SYMBOL



BATTERY AND GROUND TERMINALS FOR THIS CIRCUIT MODULE:

IC CODE	BAT TERM	GRD TERM
137C	25	11
137D	25	11
137F	25	11
137H	25	11
137H	25	11
137H	25	11

SPECIAL MANUFACTURING REFERENCES

CATEGORY	NO.
CONTROLLING DRAWING	FC200
CIRCUIT PACK CODE	FC200

SUPPORTING INFORMATION

CATEGORY	NO.
INTEGRATED CIRCUIT CODE	153A
(ANY HIGHER SERIES IS ACCEPTABLE)	3-4

FC203 CIRCUIT PACK

153A IC

2A

CPS-FC203
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BELL TELEPHONE LABORATORIES

6S

PART OF CMS 153A

CIRCUIT DESCRIPTION

A. FUNCTION

CM 153A IS USED IN THE CONVERSION BETWEEN BIPOLAR SIGNALS ON THE 3A CC 1/8 DATA LINES AND LOGIC-LEVEL SIGNALS REQUIRED BY PERIPHERAL UNIT CONTROLLER CIRCUITS (SUCH AS THE TTY CONTROLLER).

B. DETAILED DESCRIPTION

LEADS HAVING DESIGNATIONS THAT END IN 1 ARE HIGH WHEN ACTIVE, OR IN THE ONE STATE. LEADS HAVING DESIGNATIONS THAT END IN 0 ARE LOW WHEN ACTIVE, OR IN THE ONE STATE. FLIP-FLOPS ARE SET TO THE ONE STATE AND CLEARED TO THE ZERO STATE.

BIPOLAR TO LOGIC LEVEL CONVERSION

THE CONTROLLER-RECEIVED DATA LINE IS TRANSFORMER-COUPLED TO CM 153A OR LEADS AT A AND B1 FROM CDD, AND C1 AND D1 FROM CC1. THE DATA IS OR'ED BY GATES A0A AND C0A AT TC12L0, AND BY GATES B0A AND D0A AT TC12L0. THE RELATIONSHIP BETWEEN THE BIPOLAR DATA, THE INPUT TO CM 153A, AND ITS LOGIC-LEVEL DATA (CDD) AND TIMING (SHIFT) OUTPUT SIGNALS, IS SHOWN IN FIG. 1. THE LOGIC STATE OF THE BIPOLAR DATA BIT IS DETERMINED BY THE ORDER OF ITS POSITIVE AND NEGATIVE EXCURSIONS. A LOGICAL ONE IS A POSITIVE PULSE FOLLOWED BY A NEGATIVE LOBE. A LOGICAL ONE IS A POSITIVE LOBE FOLLOWED BY A NEGATIVE LOBE. CLIPPING CIRCUITS, WHICH ARE PART OF GATES WHICH MATCH THE A1, B1, C1 AND D1 INPUTS CORRECTLY, LIMIT THE NEGATIVE EXCURSION AT THIS POINT, AND PREVENT RECOVERY PROBLEMS IN THESE STATES.

THE INPUT DATA LEAD (DDO) IS SET AT THE LEADING EDGE OF THE FIRST LOBE. THE TIMING SIGNAL, IS THE TRAILING EDGE OF SHIFT WHICH OCCURS AT THE TRAILING EDGE OF THE SECOND LOBE. THUS, THE CONTROLLER IS SIGNALLED TO SAMPLE THE INCOMING DATA IN THE CENTER OF THE BIT PERIOD WHEN THE DATA LEAD IS STABLE. CARE HAS BEEN TAKEN TO MINIMIZE THE NUMBER OF GATES THAT CONTROL THE DDO AND SHIFT LEADS IN ORDER THAT VARIATIONS IN GATE DELAYS WILL NOT DESTROY THE RELATIONSHIP BETWEEN THE SIGNALS. MAXIMUM TIMES FOR THE 3A CC SERIAL 1/8 DATA ARE A 150-400 BIT INTERVAL WITH 97.5-400 LOSES.

THE SHIFT LEAD IS CONTROLLED BY GATES A0B, B0B, C0B, AND D0B, AND FLIP-FLOPS 12L1 AND 12L2. INITIALLY, NONE OF THE GATES ARE ACTIVE AND BOTH FLIP-FLOPS ARE IN THE CLEARED STATE SO THAT SHIFT IS HIGH. IF INZED AND INWED ARE NOT ACTIVE, THE FIRST LOBE OF THE INPUT DATA BIT WILL ACTIVATE ONE OF THE GATES (DEPENDING ON WHETHER THE BIT IS A ONE OR ZERO AND IF IT IS FROM CDD OR CC1) AND PULL SHIFT LOW. THE FIRST LOBE WILL ALSO ACTIVATE ONE OF THE GATES FORMING TC12L0 OR TC12L0 WHICH WILL SET ONE OF THE FLIP-FLOPS, 12L1 OR 12L2, DEPENDING ON CONDITIONS PREVIOUSLY DESCRIBED. THE PURPOSE OF THESE FLIP-FLOPS IS TO HOLD SHIFT LOW DURING ANY GAP THAT MIGHT BE PRESENT BETWEEN THE FIRST AND SECOND LOBES AND TO PREVENT THE SECOND LOBE FROM CHANGING THE STATE OF THE DATA FLIP-FLOP (D).

WHEN THE SECOND LOBE OF THE INCOMING DATA BIT IS ACTIVE THE RATE OF THE GATE ACTIVATED BY THE FIRST LOBE WILL ACTIVATE IT AND IT WILL ALSO HOLD SHIFT LOW (A0B AND B0B ARE MATES AS ARE C0B AND D0B). THIS LOBE WILL ALSO SET THE FLIP-FLOP LEAD OR 12L1 THAT MAY NOT SET BY THE FIRST LOBE. WHEN THE SECOND FLIP-FLOP IS SET, IT INHIBITS THE PATH BY WHICH THE FIRST FLIP-FLOP HELD SHIFT TO GROUND, WHEN THE FIRST LOBE IS OVER ONLY THE GATE ACTIVATED BY THE SECOND LOBE HOLDS SHIFT LOW.

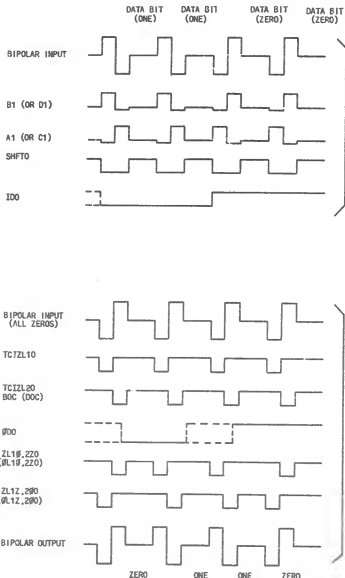
WITH BOTH FLIP-FLOPS SET, THE INPUT TO CDD FROM B01 IS HIGH. THE OTHER INPUTS TO CDD, TC12L1 AND TC12L0 ARE CONTROLLED BY THE DATA LOBES. WHEN THE FIRST LOBE IS GONE, ONLY THE SECOND LOBE CONTROLS CDD. WHEN THE SECOND LOBE EXPIRES, THE GATE HOLDING SHIFT IS DISABLED AND SHIFT WILL GO HIGH. CDD WILL GO LOW AT THIS TIME AND CLEAR BOTH FLIP-FLOPS. CDD ALSO BLOCKS THE 12L1 AND 12L2 CONNECTION TO SHIFT SO THAT FALSE SIGNALS CANNOT OCCUR ON THIS LEAD AS THE FLIP-FLOPS CHANGE FROM THE 11 TO THE 00 STATE.

LEAD DDO IS CONTROLLED BY THE D FLIP-FLOP. DDO RETAINS THE LAST INCOMING DATA STATE UNTIL IT IS UPDATED BY THE FIRST LOBE OF A NEW DATA BIT. IF THE NEW DATA BIT IS A ZERO, TC12L0 WILL BE ACTIVE FIRST AND DRIVE GATE 12L101 HIGH. TERMINALS 19 AND 23 ARE EXTERNALLY TIED TOGETHER SO THAT DDOA AND DDOB BOTH BECOME HIGH. IT SHOULD BE NOTED THAT 12L1 AND 12L2 ARE INITIATED FROM THE CLEARED STATE AND THAT TC12L0 SETS 12L1 BUT DOES NOT AFFECT 12L2. DDOA WILL PULL TC12L0 LOW, WHICH WILL CLEAR DDO AND DRIVE DDO HIGH, TO ITS ZERO STATE. WHEN THE SECOND LOBE IS ACTIVE FOR THE ZERO DATA BIT, TC12L0 WILL DRIVE 12L201 HIGH. HOWEVER, 12L1 WAS SET BY THE FIRST LOBE, IN ORDER TO PREVENT 12L201 FROM CHANGING THE D FLIP-FLOP.

IF THE INCOMING DATA BIT IS A ONE, TC12L0 WILL BE ACTIVE FIRST. 12L201 WILL BE HIGH WHILE 12L1 IS CLEARED, AND THE D FLIP-FLOP WILL BE SET. DDO WILL THEN BE LOW, WHICH IS THE ONE STATE. WHEN THE SECOND LOBE IS ACTIVE FOR AN INCOMING ONE, TC12L1 IS ACTIVE, AND WILL DRIVE 12L101 HIGH. TC12L0, HOWEVER, WILL HAVE SET 12L2, WHICH PREVENTS DDOA FROM CHANGING D.

FIG. 1
BIPOLAR TO LOGIC
LEVEL CONVERSION
USING CM 153A

FIG. 2
LOGIC LEVEL TO
BIPOLAR CONVERSION
USING CM 153A



LEADS ZACTD AND BACTD INDICATE WHICH, IF ANY, CC IS ACTIVELY COMMUNICATING WITH THE CONTROLLER. THE ACT FLIP-FLOP, FORMED BY GATES ACTD AND ACT1, IS SET BY GATES B0C ON DDO TO INDICATE THAT ONE OF THE CC'S IS SUPPLYING INPUT DATA. FLIP-FLOP ACT1 IS SET BY B0C WHEN CC IS ACTIVE, A IS CLEARED BY D0C WHEN CC1 IS ACTIVE. THE ACT AND ACT1 FLIP-FLOPS ARE COMBINED TO ACTIVATE ZACTD WHEN CC IS ACTIVE AND BACTD WHEN CC1 IS ACTIVE. BOTH THE ZACTD AND BACTD ARE HIGH WHEN NEITHER CC IS ACTIVE.

INZED AND INWED BLOCK INPUT DATA FROM CDD AND CC1 WHEN THEY ARE ACTIVE.

LEAD IDPO WILL BE ACTIVE WHEN EITHER LOBE OF THE INPUT DATA BIT IS PRESENT. IT CAN BE USED BY AN EXTERNAL CIRCUIT TO INDICATE WHEN INCOMING DATA IS PRESENT. THE EXTERNAL CIRCUIT MUST HAVE SUFFICIENT FILTERING TO HOLD OVER ANY GAP BETWEEN LOBES.

INPUT IDPO IS USED TO INITIALIZE THE 12L1 AND 12L2 TO THE 00 STATE, AND TO CLEAR THE ACT FLIP-FLOP. THIS SIGNAL MAY BE ACTIVATED BY AN EXTERNAL CIRCUIT AT THE END OF A DATA COMMUNICATION.

LOGIC LEVEL TO BIPOLAR CONVERSION

THE 3A CC HOLDS THE DATA PORTION OF A COMMUNICATION TO A PERIPHERAL UNIT WITH AN ALL-ZEROS BIT STREAM. THIS BIT STREAM IS USED BY THE PERIPHERAL UNIT AS BIT TIMING FOR THE BIPOLAR DATA SENT TO THE 3A CC. THE 3A CC MAINTAINS THE ALL-ZEROS BIT STREAM UNTIL IT RECEIVES A REPLY FROM THE PERIPHERAL UNIT, OR UNTIL THE MAXIMUM INTERVAL IN WHICH IT SHOULD RECEIVE A REPLY IS EXCEEDED. THUS, FOR EACH OUTGOING BIT PERIOD, LEAD A1 IS ACTIVELY FOLLOWED BY B1 ACTIVE. INPUTS ENBDO AND ENWDO ARE ACTIVATED TO START THE OUTPUT AND DIRECT IT TO CDD OR CC1.

GATES AL1B, Z2D AND AL1C, Z2D ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CDD. GATES AL1B, Z2D AND AL1C, Z2D ARE TRANSFORMER-COUPLED TO THE OUTGOING DATA LINE TO CC1. THESE GATES ARE HELD HIGH WHEN THERE IS NO INCOMING DATA OR WHEN THE SIGNAL LEAD (EXZED, ENWED) IS NOT ACTIVE.

THE RELATIONSHIP BETWEEN THE ALL-ZEROS INPUT DATA, THE LOGIC LEVEL OUTGOING DATA LEAD, AND THE BIPOLAR OUTPUT DATA, IS SHOWN IN FIG. 2. THE LOGIC LEVEL OUTGOING DATA SIGNAL (D0C) IS TROGLED INTO B0B PRIOR TO THE BIT PERIOD. THE OUTPUT OF B0B IS ACTIVELY FOLLOWED BY THE SIGNALS DERIVED FROM THE INCOMING DATA (TC12L1 AND TC12L0) TO DETERMINE THE ORDER IN WHICH TC12L1, Z2D AND TC12L0, Z2D WILL BE ACTIVE. IF A ONE IS TO BE SENT, TC12L1, Z2D WILL BE ACTIVE DURING THE FIRST LOBE AND TC12L0, Z2D WILL BE ACTIVE DURING THE SECOND LOBE. THE RELATIONSHIP BETWEEN THE LOGIC LEVEL OUTGOING DATA AND THE BIPOLAR OUTPUT DATA WILL BE THE INVERSE OF THE ENABLED OUTPUT GATES ZL1B, Z2D AND ZL1C, Z2D AND AL1B, Z2D AND AL1C, Z2D.

A GATE IN EACH PAIR IS CONNECTED TO THE OPPOSITE END OF THE PRIMARY OF A TRANSFORMER. EACH PAIR OF GATES IS PROVIDED WITH A TRANSFORMER. THE ORDER IN WHICH THE GATES ARE ACTIVELY FOLLOWED BY THE POLARITY OF THE PULSE AVAILABLE AT THE TRANSFORMER SECONDARY WINDING. THE STATE OF THE DATA LEAD IS TROGLED INTO B0B BY B0C (OR D0C) DURING THE BIT INTERVAL PRECEDING THAT IN WHICH THE BIT IS TRANSMITTED. INPUTS SBDOA AND SBDOB ALLOW DIRECT SET AND CLEAR OPERATIONS ON B0B.

SYMBOL LEAD

C. PINNINGS

PINNINGS	FUNCTION
ACTP	SET OR CLEAR TO DETERMINE WHICH INPUT PORT IS ACTIVE
ACT1	SET AND CLEAR INPUT PORT IS ACTIVE
B1	INPUTS FROM CDD
CDD	CLEAR DDO FF
D1	INPUTS FROM CC1
ENBDO	ENABLE OUTPUT TO CDD
ENWDO	ENABLE OUTPUT TO CC1
ID	INCOMING DATA
IDPO	INCOMING DATA OVER, INPUT
12L1	INCOMING DATA PRESENT
12L2	INCOMING ZERO LOBE SET BY FIRST LOBE WHEN INPUT IS ZERO
12L2	INCOMING DATA
BACTD	CC1 IS ACTIVE
B0B	OUTGOING DATA
AL1B, Z2D	OUTGOING DATA BIT
AL1C, Z2D	FIRST LOBE FOR A ONE, SECOND LOBE FOR A ZERO TO CDD
SHFT	FIRST LOBE FOR A ZERO, SECOND LOBE FOR A ONE TO CC1
SBDOA	SET B0B FF
SBDOB	CDD IS ACTIVE
ZL1B, Z2D	FIRST LOBE FOR A ONE, SECOND LOBE FOR A ZERO TO CDD
ZL1C, Z2D	FIRST LOBE FOR A ZERO, SECOND LOBE FOR A ONE TO CC1

FC205 CIRCUIT PACK

BELL TELEPHONE LABORATORIES

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CPS-FC203

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